Fermilab

HRM-II Digital I/O

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General Description

The Digital I/O module interfaces 64 bits of digital I/O through the use of 8, 8 bit wide R/W data registers. Each register is individually addressable and can be configured as input or output port by writing to an internal 8 bit data direction register.

Two bytes of digital data are connected each of four 37-pin D type connectors accessible from the back panel. Data transfer is into the module is word wide. I/O data transfer is byte wide. In addition to the I/O ports, two Form C relays are accessible through two, 3-pin Phoenix headers, also on the back panel. With the exception of the relays, all I/O is non-isolated. Each output can sink up to 64mA and source up to 32mA. Inputs are TTL compatible with input current of +/-20uA.

Three actions will clear all registers and set the I/O ports to all input: 1) A reset generated from power up, 2) Resetting the HRMII, 3) Local onboard reset via a tact switch.

Board Address Space

Base + 0x00, Read-only
Module ID Register

15 8	7 0
Module ID = 0x4E	Module Revision Number = 0x01

Base + 0x01, Read/Write
Test Register

15 8	7 0
x	Test

Base + 0x02, Read/Write, Relay 0 Register
Base + 0x03, Read/Write, Relay 1 Register

15 1	0
x	Relay On

Base + 0x04, Read/Write
Data Direction Register

15 8	7	6	5	4	3	2	1	0
x	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

0=all bits input, 1=all bits output
Base + 0x05 through Base + 0x17 Not Used

Base + 0x18 through 0x1F, Read/Write
Ports 0 through 7

15 8	7	6	5	4	3	2	1	0
x	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

Address to Connector Mapping

Port Address	Controlled by DDR (0x04) Bit	IO Connector (LSB---MSB)	Strobe Output	Direction Output
0x18	0	P4-1 through 8	P4-19	P4-37
0x19	1	P4-9 through 16	P4-18	P4-37
0x1A	2	P3-1 through 8	P3-19	P3-37
0x1B	3	P3-9 through 16	P3-18	P3-37
0x1C	4	P2-1 through 8	P2-19	P2-37
0x1D	5	P2-9 through 16	P2-18	P2-37
0x1E	6	P1-1 through 8	P1-19	P1-37
0x1F	7	P1-9 through 16	P1-18	P1-37

Signal Names and Descriptions

HRM-II Bus Signals

D15-D0	Bi-directional	Data
/RD	Input	Read strobe
/WR	Input	Write strobe
A15-A0	Input	Address
CLK	Input	40 Mhz
/RESET	Input	System reset
/RDY*	Output	Board ready for new cycle.

* /RDY is active on the falling edge.

I/O Signals

STB07-STB00	Output	100ns positive pulse. Output data is valid on falling edge.
DIR03-DIR00	Output	Data direction for the port accessed. Active on the falling edge of STB
B8-B0	Bi-directional	Bit 8 – 0

Register Descriptions and Operation

Board ID

A 16 bit read-only register resides in an EPM3256 FPGA. It is set to 0x4E01.

Data Direction Register (DDR)

Ports are programmable by writing to the DDR. Writing the register stores the low 8 bits of a 16-bit word. The LS bit represents I/O port 0. Setting a bit programs the associated port as an output. All bits are cleared to 0 (input) upon reset. A series of LED's are onboard to reflect the current state of each port. Green indicates the port is programmed as input, red indicates an output port. These LED's are a diagnostic aid and are not viewable from outside the cabinet.

Data Registers

Data is stored by writing to a 16 bit bi-directional transceiver configured as two eight bit transceivers. Onboard D type flip-flops make up each data register. The result of writing to a data register depends on the configuration of the port associated with the register. If the port is configured as an output, data is stored and the output drivers enabled. If the port is configured as an input no action is taken. Reading a data register that is configured as an output always reads the state of the connector pin and not the state of the output latch.

Relay Registers

Each register is a single bit in D0. Setting the bit will activate the relay, clearing it will deactivate it. The bit must remain set to hold the relay energized.

Test

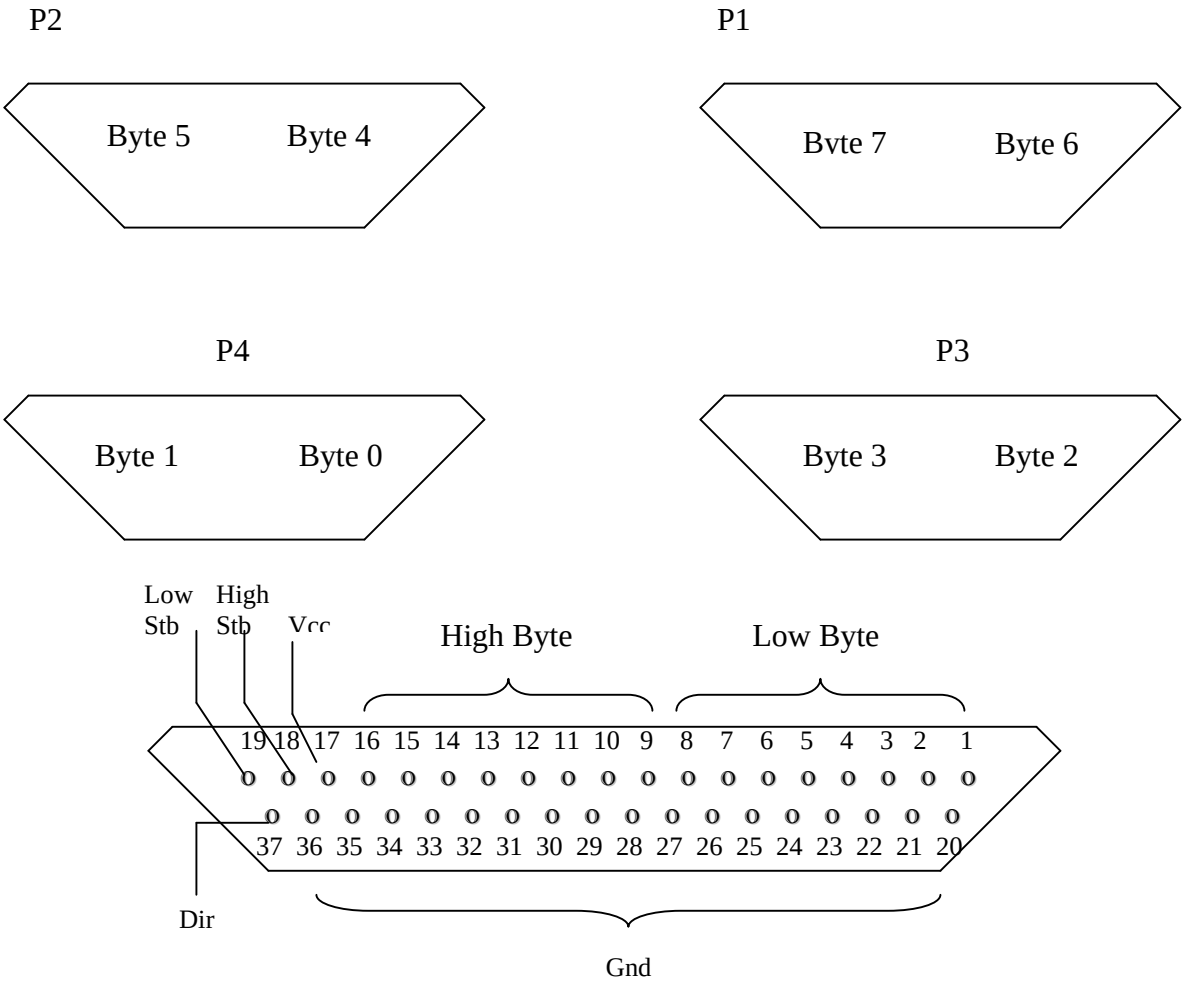
The test register is an 8 bit read/write port.

Form C Relays

Each relay has a maximum rating of 1 amp at 110v. The operating function of each relay is single side stable. Writing a 1 to a relay register will turn on the relay. The relays are not of the latching type; therefore the relay coil must remain energized for the relay to operate. Writing a 0 to a register will deenergize the relay.

Connector Pinouts

Each 37 pin D connector is associated with 2 bytes of I/O. There are 3 additional output signals. There are two strobes for each of the two bytes and one direction signal for both bytes. If direction = 0 the port being accessed is an output. Only 1 byte is accessible at a time so strobe and direction signals must be used together to select the proper byte.



HRM-II Digio Revision D Notes
15March2005

- Altera file corrections made and up-to-date, version 2:08P 3-15-2005
- Schematic file corrections made and up-to-date Tues 3-15-2005
- Digio BOM scrubbed and up-to-date 3-15-05
- No cuts, jumps, or other mutilations to Rev D PCB. May require a temporary jumper from JP2-4 to +5V for Altera programming (depends on download cable being used)

For next pass Rev E:

- Change U3 footprint to wide SOIC (DW) to allow use of 74AC541DW
- Move P3,P4 mounting holes away from back edge of board
- Add VCC jumper to JP2-4
- Move J1 and J2 closer to back edge of board so that plugs can fit properly

Other notes:

- All modules must use the same stack D connectors from the same vendor to ensure that distance from PCB pads to the face of the socket is always the same.
- The cut-out in the back panel for J1 and J2 has to be enlarged to the right (viewed from the rear of the assembled unit to provide more clearance for J2.